

TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT (Under 37 CFR 1.97(b) & 1.97(c))			Docket No. BUR920030122US1
In Re Application Of: DITLOW ET AL.			
Serial No. 10/707,286	Filing Date 12/03/2003	Examiner UNASSIGNED	Group Art Unit UNASSIGNED
Title: AUTONOMIC GRAPHICAL PARTITIONING			
<p>Address to: Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450</p> <p>37 CFR 1.97(b)</p> <p>1. <input checked="" type="checkbox"/> The Information Disclosure Statement submitted herewith is being filed within three months of the filing of a national application other than a continued prosecution application under 37 CFR 1.53(d); within three months of the date of entry of the national stage as set forth in 37 CFR 1.491 in an international application; before the mailing of a first Office Action on the merits, or before the mailing of a first Office Action after the filing of a request for continued examination under 37 CFR 1.114.</p> <p>37 CFR 1.97(c)</p> <p>2. <input type="checkbox"/> The Information Disclosure Statement submitted herewith is being filed after the period specified in 37 CFR 1.97(b), provided that the Information Disclosure Statement is filed before the mailing date of a Final Action under 37 CFR 1.113, a Notice of Allowance under 37 CFR 1.311, or an Action that otherwise closes prosecution in the application, and is accompanied by one of:</p> <p><input type="checkbox"/> the statement specified in 37 CFR 1.97(e);</p> <p>OR</p> <p><input type="checkbox"/> the fee set forth in 37 CFR 1.17(p).</p>			

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AUTONOMIC GRAPHICAL PARTITIONING**Payment of Fee**

(Only complete if Applicant elects to pay the fee set forth in 37 CFR 1.17(p))

- ☐ A check in the amount of _____ is attached.
- ☒ The Director is hereby authorized to charge and credit Deposit Account No. 09-0456 as described below.
- ☐ Charge the amount of _____
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Signature

Dated: 2/16/04

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CC:



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of

Ditlow et al.

Serial No.: ~~Not Yet Assigned~~ 10/707,286 Group Art Unit: Unknown

Filing Date: ~~Concurrently Herewith~~ 12/03/03 Examiner: Unknown

For: AUTONOMIC GRAPHICAL PARTITIONING

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

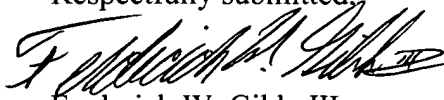
Sir:

Under the provisions of 37 CFR §1.97 through §1.99 and pursuant to applicants' duty of disclosure under 37 CFR §1.56, applicants respectfully bring the following documents, listed on the attached form PTO-1449, to the attention of the Examiner in charge of the above-identified application. Copies of the listed documents are provided herewith for the convenience of the Examiner. This citation does not constitute an admission that the references are relevant or material to the claims. They are only cited as constituting related art of which the applicants are aware.

It is respectfully requested that the listed references be considered by the Examiner and formally made of record in this application.

Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 09-0456.

Respectfully submitted,


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INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Docket Number (Optional)

BUR920030122US1

Application Number 10/707,286

~~Not Yet Assigned~~

Applicant(s)

Ditlow et al.

Filing Date

12/03/03

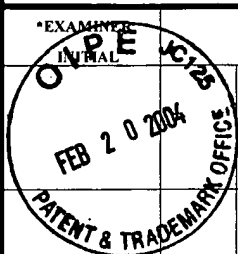
~~Concurrently Herewith~~

Group Art Unit

Not Yet Assigned

*EXAMINER

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)



"An Analytical Approach to Floorplanning for Hierarchical Building Blocks Layout", IBM Technical Disclosure Bulletin, Vol. 33, No. 6A, Nov. 1990, pp. 164-165.

Ying et al., "An Analytical Approach to Floorplanning for Hierarchical Building Blocks Layout", IEEE Transactions on Computer-Aided Design", Vol. 8, No. 4, April 1989, pp. 403-412.

Yamada et al., "A Block Placement Method Based on Balloon Model", IEEE International Symposium on Circuits and Systems, Vol. 3, 1990, 1680-1683.

G. Vijayan, "Overlap Elimination in Floorplans", Proceedings Fourth CSI/IEEE International Symposium on VLSI Design, 1991, PP. 157-162.

Choi et al., "A Floorplanning Algorithm Using Rectangular Voronoi Diagram and Force-Directed Block Shaping", International Conference on Computer-Aided Design, Nov. 1991, pp. 56-59.

EXAMINER

DATE CONSIDERED

*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.